REMARKS

Claims 1-24 are all the claims pending in the application.

In response to the Amendment filed May 5, 2003, the Examiner removed all of the previous rejections. Now, the status of the claims is the following.

Claims 1-4, 11-14, and 21 are rejected under 35 U.S.C. § 102(e) as being anticipated by newly-cited Mutoh (US 5,940,101, hereafter "Mutoh '101"). Claims 7 and 17 are rejected under 35 U.S.C. § 102(e) as being anticipated by newly-cited Woodworth (US 5,991,041). Claims 5, 6, 15, 16, and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Mutoh '101 in view of newly-cited Mutoh (US 5,583,552, hereafter "Mutoh '552"). Claims 8-10, 18-20, 23, and 24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Woodworth in view of Mutoh '552. Applicant respectfully traverses the claim rejections with the following comments.

Mutoh '101 relates to a method and apparatus for determining optimum ink drop formation frequency in an ink jet printer. FIG. 1 of the reference shows an example of the apparatus, including: a reference oscillator CG for generating a reference clock signal CLK of an oscillation frequency instructed from an MPU 10, a frequency divider FD for dividing the frequency of the reference clock signal CLK by N (positive integer) to produce an excitation signal PCLK, a delayed pulse generator DG for delaying the excitation signal PCLK to N (positive integer) stages in response to the reference clock signal CLK to produce pulse trains θ_0, θ_1, θ_2, . . . θ_{N-1}, a multiplexer (2) MP2 for selecting one of the delayed pulse trains θ_0, θ_1, θ_2, . . . θ_{N-1}, an oscillation element driver VD for driving the oscillator 3 with the pulse signal selected by the multiplexer (2) MP2, a pulse width modulator PM for converting image data into a pulse width signal corresponding to a density gradation, a probe pulse generator PG for generating a

probe pulse signal having a pulse width sufficiently shorter than the period of the excitation signal PCLK in synchronism with a rising or falling edge of the excitation signal PCLK, and a synchronizing circuit SC for synchronizing a rising or falling edge of the output of the pulse width modulator PM with a rising or falling edge of the excitation signal PCLK from the frequency divider FD.

Mutoh '552 relates to an ink jet recording apparatus of the continuous jet type wherein ink is jetted continuously from a nozzle of an ink jet recording head.

Woodworth relates to a method and apparatus for measuring dimensions of objects on a conveyor.

Rejection of claims 1-4, 11-14, and 21:

Applicant submits that Mutoh '101 does not teach or suggest all of the limitations of claims 1-4, 11-14, and 21. Claim 1 recites a pulse width modulating signal output device which makes a pulse of a pulse width modulating signal rise synchronously with one of a first clock signal and a processing clock signal generated by an operation device, and makes the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the processing clock signal generated by the operation device. Applicant submits that Mutoh '101 fails to disclose this feature of the claims.

The reference discloses "a synchronizing circuit SC for synchronizing a rising or falling edge of the output of the pulse width modulator PM with a rising or falling edge of the excitation signal PCLK from the frequency divider FD." Col. 1, lines 55-58. However, this disclosure does not correspond to the claimed pulse width modulating signal output device. In particular, claim 1 requires that a pulse width modulating signal rise synchronously with one of a first clock

signal and a processing clock signal generated by an operation device, and makes the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the processing clock signal generated by the operation device. Clearly, Mutoh '101 fails to make such a disclosure, since the disclosure pertains to a single frequency divided clock pulse.

Thus, claim 1 and its dependent claims 2-4 and 21 are not anticipated by Mutoh '101.

Furthermore, claim 11 and its dependent claims 12-14 are not anticipated by Mutoh '101, for an analogous reason to that described above for claim 1.

Rejection of claims 7 and 17:

Applicant submits that Woodworth does not teach or suggest the pulse width modulating signal output device which makes a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the processing clock signal generated by the operation device, and makes the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the processing clock signal generated by the operation device, as claimed in claim 7. The Examiner refers to col. 6, lines 31-44; col. 8, lines 56-65; and col. 10, lines 59-67; with respect to this feature of the claim, but none of the cited portions of the reference disclose the aforementioned feature of claim 7. Instead, Woodworth only generally discloses using synchronized pulse width modulation, without specifically teaching or suggesting all of the limitations of claim 7, including the interoperations of a clock signal and phase-shifted version of the clock. Therefore, claim 7 is not anticipated by Woodworth.

Also, claim 17 is not anticipated by Woodworth for an analogous reason to that for claim 7.

Rejection of claims 5, 6, 15, 16, and 22:

Applicant submits that claims 5, 6, 15, 16, and 22 are allowable over the prior art, at least because Mutoh '552 fails to make up for the above-noted deficiencies of Mutoh '101. The Examiner asserts that in the synchronizing circuit SC, a picture element recording clock DCLK is produced, which has rising and falling edges synchronized with rising edges of a registration adjusting clock SCLK and an exciting clock PCLK, respectively, as seen in FIG. 6. However, as shown in FIG. 6, DCLK* has its rising and falling edges lined up with the rising edge of PCLK, but neither the rising edge nor the falling edge of DCLK* lines up with the rising or falling edges of SCLK*. Also, in the discussion of synchronizing, col. 17, lines 10-24 of Mutoh '552 only discloses a synchronizing circuit SC for synchronizing a rising or falling edge of an output of the pulse width modulator PWM with a rising or falling edge of the exciting clock signal PCLK. Such a disclosure in Mutoh '552 falls short of teaching or suggesting the above-identified features claims 1, 7, 11, and 17, which Mutoh '101 also fails to disclose. Hence, claims 5, 6, 15, 16, and 22 are allowable over the prior art.

Rejection of claims 8-10, 18-20, 23, and 24:

Applicant submits that claims 8-10, 18-20, 23, and 24 are allowable over the prior art, at least because Mutoh '552 fails to make up for the above-described deficiencies of Woodworth.

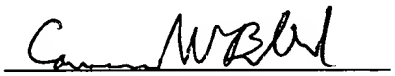
Additionally, the rejections of claims 5, 6, 15, 16, and 22 and claims 8-10, 18-20, 23, and 24 are deficient, because the Examiner has failed to identify a suggestion or motivation to combine the references. At a minimum, Woodworth and Mutoh '101, Mutoh '552 comprise non-analogous art, since they relate to operations of a conveyor mechanism, and ink jets printers.

Since the timing issues of these fields are different from each other and also different from those of the invention, the references may not be properly combined against the pending claims.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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